A SYSTEM AND METHOD FOR MULTIPLE CYCLE CAPTURE OF CHIP STATE

ABSTRACT OF THE DISCLOSURE

Test circuitry is incorporated on a chip die together with a circuit to be tested, such as an ASIC or microprocessor, to provide external access to signals that are internal to an integrated circuit chip package. A test device includes a state machine responsive to (i) an arm command for transitioning from a standby state to an armed state, (ii) a final trigger event for transitioning from the armed state to a triggered state, and (iii) a post trigger count event for transitioning from the triggered state to the standby state. A controller provides the arm command and issues appropriate configuration controls to collect signal samples. In particular, a network responds to these commands from the controller to selectively provide signal samples from a device under test. A trigger event generator responds to logic or other characteristics of the signal samples to provide trigger events. These trigger events are counted by a trigger event counter in the armed state of the state machine to identify the final trigger event corresponding to an occurrence of a programmable number of the trigger events. A store event generator also responds to a programmed characteristic or combination(s) of the signal samples to provide a store event. Either or both of the event generators may use a mask to provide these events. A post trigger sample counter operates in the triggered state to provide the post trigger count event in response to a programmable number of signal samples being captured. A memory operates in the triggered state to store the samples being captured. The memory may optionally store samples in the armed state which occur prior to the targeted samples so as to provide test data from cycles prior to the targeted events.